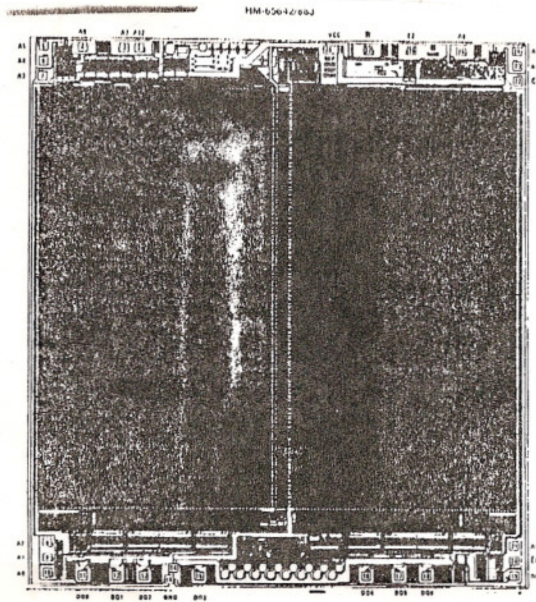
Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Metallization Topology

DIE DIMENSIONS:
276.8 x 305 5 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ + 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness. 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature. Ceramic DIP - 460°C (Max)
Ceramic LCC - 460°C (Max)

WORST CASE CURRENT DENSITY:
0.9×10^5 A/cm^2

Metallization Mask Layout

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref:
Bond Pads : .004 min

APPROVED BY: CB	**DIE SIZE: .276" x .305"**	**DATE: 2/6/01**
MFG: Harris	**THICKNESS: .019"**	**P/N: HM-65642**